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Date : September 27, 2005

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Re: Our Docket No. 60417 (71987)
U.S. Serial No. 10/728,304

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Docket No. 60417 (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: C. Chen et al.

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U.S. SERIAL NO.: 10/728,304

EXAMINER: T. Nguyen

SEP 27 2005

FILED: December 3, 2003

GROUP: 2829

FOR: CHIP CARRIER AND METHOD FOR TESTING ELECTRICAL
PERFORMANCE OF PASSIVE COMPONENTCERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted by facsimile to the U.S. Patent & Trademark Office by facsimile number 571-273-8300 on September 27, 2005.

By: 
Steven M. Jensen

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO OFFICE ACTION

Applicants are in receipt of the Office Action dated June 27, 2005 of the above-referenced application. Applicants respond to the Office Action as follows.

Applicants' claimed invention is directed to a chip carrier and a method for testing electrical performance of a passive component that is serially connected to a conductive trace of the chip carrier.

C. Chen et al.
U.S. Serial No. 10/728,304
Page 2 of 4

As recited in claims 1 and 8, the chip carrier includes a first trace connected with the passive component, where the first trace has a first predetermined position and is electrically connected to a first ball pad. The chip carrier further includes a second trace not connected with the passive component, where the second trace has a second predetermined position located on the same surface as the first predetermined position, and the second trace is electrically connected to a second ball pad located on the same surface as the first ball pad. The first and second predetermined positions are exposed from a solder mask layer applied on the chip carrier.

The above-described arrangement allows the exposed first and second predetermined positions to be electrically connected by an electrically conductive material to form a short circuit, such that the first and second ball pads on the same surface serve as test points contacted by test heads to perform an electrical performance test.

Claims 1-7 were rejected under 35 USC 102(a) as being anticipated by U.S. Patent 6,577,490 to Ogawa et al. ("Ogawa"). Claims 8 and 11-17 were rejected under 35 USC 103(a) as being unpatentable over Ogawa in view of "Admitted Prior Art" (APA). Claims 9 and 10 were rejected under 35 USC 103(a) as being unpatentable over APA in view of U.S. Patent 5,698,895 to Pedersen et al. These rejections are respectfully traversed.

It is noted that the Ogawa patent is not prior art to the subject application under 35 USC 102(a). Ogawa was patented on June 10, 2003. However, Applicants have claimed priority to Taiwan Application 092107226, filed on March 31, 2003, which predates the issue date of the Ogawa patent.

Ogawa does not teach or suggest a chip carrier or a method *for testing electrical performance of a passive component* that is serially connected to a conductive trace of the chip carrier. In particular, there is no teaching or suggestion that two ball pads located on the same surface serve as test points contacted by test heads to perform an electrical performance test.

C. Chen et al.
U.S. Serial No. 10/728,304
Page 3 of 4

Ogawa is directed to a wiring board for simplifying connections of electronic parts mounted on a principal face side of the wiring board and chip capacitors mounted on a reverse face side therof (see, e.g., column 1, lines 40-44). There is simply no teaching or suggestion of a chip carrier and a method for testing electrical performance of a passive component.

On pages 2-3 of the Office Action of 06/27/2005, it was alleged that Ogawa discloses a first predetermined position ("under 122") and a second predetermined position ("under 930" in FIG. 16). However, these positions shown in FIG. 16 of Ogawa are not located on the same surface and are not exposed from a solder mask layer, as required in claims 1 and 8. Moreover, there is no teaching or suggestion in Ogawa that the position "under 122" and the position "under 930" are to be electrically connected by an electrically conductive material to form a short circuit for an electrical performance test.

Also on pages 2-3 of the Office Action, it was alleged that a capacitor-connecting pad 949 shown in FIG. 16 of Ogawa is equivalent to Applicants' claimed "first ball pad," and a wiring layer 927 is equivalent to the claimed "second ball pad." However, reference numerals 949 and 927 are not ball pads. There is no teaching or suggestion in Ogawa that two ball pads located on the same surface serve as test points contacted by test heads to perform an electrical performance test.

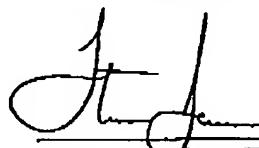
Regarding independent claim 8, the Applicants' claimed invention was distinguished from "APA" in the response filed on April 1, 2005. Moreover, FIGS. 7A, 7B, and 8 and the Background of the Invention section of the application do not teach or suggest first and second predetermined positions located on the same surface and exposed from a solder mask layer, or first and second ball pads located on the same surface as test points contacted by test heads. Therefore, "APA" could not be combined with Ogawa to somehow produce the Applicants' claimed invention.

C. Chen et al.
U.S. Serial No. 10/728,304
Page 4 of 4

For at least the reasons discussed above, Ogawa and "APA", whether taken alone or in combination, do not anticipate or otherwise render obvious the Applicants' claimed invention. Therefore, independent claims 1 and 8, and dependent claims 2-7 and 9-17 are patentable over Ogawa and "APA".

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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